FIN-BASED DOUBLE POLY DYNAMIC THRESHOLD CMOS FET WITH SPACER GATE AND METHOD OF FABRICATION

Abstract of the Disclosure

The present invention provides a dynamic threshold (DT) CMOS FET and a method for forming the same that results in improved device performance and density. The preferred embodiment of the present invention provides a DT CMOS FET with a short, low resistance connection between the gate and the body and with low body-to-source/drain capacitance. The low body-to-source/drain capacitance is achieved using a thin, fin-type body. The low resistance connection between the gate and the body contact is achieved by having the gate and body contact aligned on opposite long sides of the fin with a bridge over the top of the narrow fin electrically connecting the gate and body.

Figures